CLAIMS

1. A method of forming a semiconductor circuit, comprising the steps of:

forming a first transistor, comprising the steps of:

forming a first source/drain region as a first doped region in a fixed relationship to a semiconductor substrate;

forming a second source/drain region as a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

forming a first gate in a fixed relationship to the first source/drain region and the second drain region; and

forming a second transistor, comprising the steps of:

forming a third source/drain region as a third doped region in a fixed relationship to the semiconductor substrate;

forming a fourth source/drain region as a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

forming a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the steps of forming the first gate and the second gate comprise forming the first gate to comprise a first dopant concentration and forming the second gate to comprise a second dopant concentration different from the first dopant concentration.

2. The method of claim 1 wherein the steps of forming the first and the second gate further comprise:

forming a semiconductor layer in a fixed relationship to the semiconductor substrate;

in an implant step, selectively implanting dopants into a portion of the semiconductor layer in an area corresponding to the first transistor while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the second transistor.

3. The method of claim 2 wherein the steps of forming the first gate and the second gate further comprise patterning and etching the semiconductor layer to form the first gate from the area corresponding to the first transistor and the second gate from the area corresponding to the second transistor.

4. The method of claim 2 wherein the semiconductor layer comprises polysilicon.

5. The method of claim 4 wherein the step of forming a semiconductor layer comprises forming a polysilicon layer with an in-situ doping.

6. The method of claim 5:

wherein the in-situ doping comprises p-type in-situ doping; and

wherein the first, second, third, and fourth doped regions comprise n-type doped regions.

7. The method of claim 2:

wherein the first transistor has a first threshold voltage in response to the first dopant concentration; and

wherein the second transistor has a second threshold voltage in response to the second dopant concentration and such that the second threshold voltage is greater than the first threshold voltage.

8. The method of claim 7 wherein the second transistor comprises a state transistor in a memory cell.

9. The method of claim 8:

wherein the state transistor comprises a first state transistor;

and further comprising the step of forming a second state transistor in the memory cell, comprising the step of forming a third gate corresponding to the second state transistor and comprising the second dopant concentration.

10. The method of claim 9 and further comprising the steps of:

forming a first access transistor in the memory cell, the first access transistor coupled and operable to read a state from, and write a state to, a source/drain of the first state transistor; and

forming a second access transistor in the memory cell, the second access transistor coupled and operable to read a state from, and write a state to, a source/drain of the second state transistor.

11. The method of claim 10 wherein the first and second access transistors comprise source/drain regions of a conductivity type that is complementary of source/drain regions of the first and second state transistors.

12. The method of claim 11 wherein the first, second, third, and fourth doped regions comprise n-type doped regions.

13. The method of claim 12:

wherein the semiconductor layer comprises polysilicon; and

wherein the step of forming a semiconductor layer comprises forming a polysilicon layer with an in-situ doping.

14. The method of claim 12 wherein the first transistor comprises a transistor in a sense amplifier.

15. The method of claim 8 wherein the first transistor comprises a transistor in a sense amplifier.

16. The method of claim 15 wherein the first, second, third, and fourth doped regions comprise n-type doped regions.

17. A method of forming a memory configuration, comprising the steps of:

forming a plurality of memory cells, wherein each of the memory cells is formed comprising the step steps of:

forming a first transistor, comprising the steps of:

forming a first source/drain region as a first doped region in a fixed relationship to a semiconductor substrate;

forming a second source/drain region as a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

forming a first gate in a fixed relationship to the first source/drain region and the second drain region; and

forming a second transistor outside of the plurality of memory cells, comprising the steps of:

forming a third source/drain region as a third doped region in a fixed relationship to the semiconductor substrate;

forming a fourth source/drain region as a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

forming a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein, the step of forming the first gate for each cell in the plurality of memory cells and the step of forming the second gate further comprise:

forming a semiconductor layer in a fixed relationship to the semiconductor substrate; and

in an implant step, selectively implanting dopants into a portion of the semiconductor layer in an area corresponding to the second transistor such that the area has a first dopant concentration while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the first transistor in each cell.

18. The method of claim 17:

wherein, for each cell, the first transistor has a first threshold voltage in response to the implant step; and

wherein the second transistor has a second threshold voltage in response to the first dopant concentration and such that the second threshold voltage is less than the first threshold voltage.

19. The method of claim 18:

wherein the first transistor comprises a first state transistor;

and further comprising the step of forming a second state transistor in the memory cell, comprising the step of forming a third gate corresponding to the second state transistor and wherein the implant step further comprises selectively implanting dopants into a portion of the semiconductor layer while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the second state transistor in each cell.

20. The method of claim 19 and further comprising the steps of:

forming a first access transistor in the memory cell, the first access transistor coupled and operable to read a state from, and write a state to, a source/drain of the first state transistor; and

forming a second access transistor in the memory cell, the second access transistor coupled and operable to read a state from, and write a state to, a source/drain of the second state transistor.

21. A semiconductor circuit, comprising:

a first transistor, comprising:

a first source/drain region comprising a first doped region in a fixed relationship to a semiconductor substrate;

a second source/drain region comprising a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

a first gate in a fixed relationship to the first source/drain region and the second drain region; and

a second transistor, comprising:

a third source/drain region comprising a third doped region in a fixed relationship to the semiconductor substrate;

fourth source/drain region comprising a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the first gate comprises a first dopant concentration and the second gate comprises a second dopant concentration different from the first dopant concentration.

22. A memory configuration comprising:

a plurality of memory cells, wherein each of the memory cells comprises:

a first transistor, comprising:

a first source/drain region comprising a first doped region in a fixed relationship to a semiconductor substrate;

a second source/drain region comprising a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

a first gate in a fixed relationship to the first source/drain region and the second drain region; and

the memory configuration further comprising a second transistor outside of the plurality of memory cells, comprising:

a third source/drain region comprising a third doped region in a fixed relationship to the semiconductor substrate;

a fourth source/drain region comprising a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the first gate for each cell in the plurality of memory cells comprises a first dopant concentration that is less than a dopant concentration in the second gate.

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